

## ABSTRACT OF THE DISCLOSURE

1       A flexible, reconfigurable processing system architecture  
2 allows for the implementation of a variety of processing system  
3 configurations to be implemented on a single device, which is  
4 preferably a PCI bus add-in extension board with an attached  
5 daughter card attached and electrically connected thereto through  
6 a PCI Mezzanine type connector, and which is plugged into a  
7 personal computer PCI expansion slot. The architecture uses the  
8 PCI bus, for example, as the local CPU bus for an embedded  
9 processor, which not only allows for flexibility in system  
10 configuration but also allows PCI devices to be hidden from the  
11 host CPU to allow for proper system startup. The architecture  
12 further permits an embedded processing CPU to be re-booted when  
13 the secondary PCI bus host bus bridge fails to respond without  
14 affecting host CPU or other secondary PCI bus peripheral devices.  
15 The architecture provides a method of loading an embedded system  
16 CPU's local memory with operating system and diagnostic code  
17 without the use of ROM or FLASH memory. A system and method of  
18 reserving memory is also disclosed which utilizes a dummy or  
19 surrogate board with little or no functionality but which has a  
20 class code of a common device such as an Ethernet card. The  
21 primary system BIOS will read the class code and reserve memory  
22 based on the surrogate card. The driver of the non-standard card  
23 such as an embedded processor, can then use the memory space  
24 allocated to the surrogate card by the BIOS.